Efficient, 50 mV startup, with transient settling time <5 ms, energy harvesting system for thermoelectric generator

A.K. Sinha✉ and M.C. Schneider

A prototype chip fabricated in 130 nm CMOS technology, designed to extract maximum power from a thermoelectric generator (TEG) is presented. In the measurements, the TEG is modelled by a voltage source (V_{TEG}) with a series resistance of 5 Ω. The prototype is fully electric, starts from $V_{TEG} = 50$ mV and it can extract 60% (at 50 mV) to 65% (at 200 mV) of the available power. Also by using present circuit schematic, an improved transient response of 3 ms (at 50 mV) and startup voltage of 50 mV is achieved.

Introduction: A common type of sensor used to convert thermal energy to electrical energy is a thermoelectric generator (TEG) [1]. Several works have been reported to convert the output of a TEG which is typically around 50 mV to around 1 V, so that it can power any load, which can be an electronic circuit or a rechargeable battery. In this regard, DC–DC converter have been an attractive device for elevating low voltage to high voltage [2]. In low-voltage applications also, the most popular techniques for DC–DC conversion is the use of the switched capacitor method, or inductively charging a capacitor [2]. The latter is more efficient and has also been widely reported in the literature. The DC–DC converter can be self-starting, or start by external means. The startup voltage, startup time and efficiency of the converter circuit are areas of improvement. This Letter presents the circuit architecture along with formulations that can be used to extract maximum power from a TEG, with low startup voltage. It can also reduce the transient settling time compared with [1, 3].

Circuit implementation: The overall architecture of the circuit is shown in Fig. 1. The auxiliary converter is driven by a low-voltage starter (LVS, shown in Fig. 2*a*), which is a two-stage enhanced swing ring oscillator [4], which starts up at around 30 mV. The LVS also has a 12-stage Dickson charge pump (DCP) that converts the AC swing into a DC voltage used to start the first current starved ring oscillator (CSRO-1), shown in Fig. 2*b*. At the 700 mV output provided from the DCP, the CSRO-1 oscillates with a time period of 10 µs. CSRO-1 drives an auxiliary boost converter stage, which consists of an N-channel metal oxide semiconductor (NMOS) switch, a low V_t on-chip diode and an external inductor L_{AUX}. Through an external inductor, the auxiliary converter boosts the voltage at V_{DDi} node to 600 mV, the V_{DDi} node has an on-chip capacitor of 1 nF. With this capacitor value, the ripple at V_{DDi} is around 20 mV. The peripherals at V_{DDi} node consume a current of 1.5 µA at 600 mV and 4 µA at 1 V.

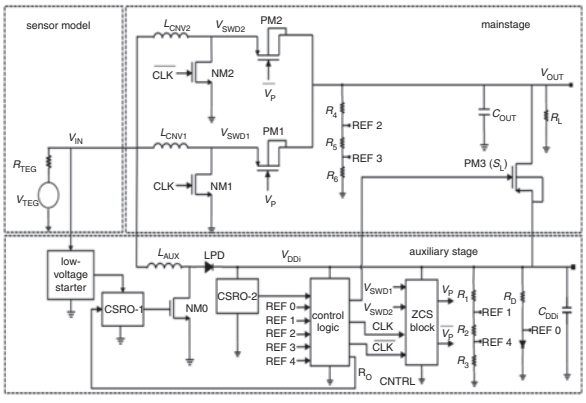

Fig. 1 *Simplified block diagram of circuit. NM0–2, are low V_t NMOS switches and PM1–3 are low V_t PMOS switches. REF0 is non-linear reference generator, and REF1–4 are node sensing networks. (W/L); NM1, 2: 480 × 4 µm/0.12 µm, PM1, 2: 120 × 4 µm/0.12 µm, NM0: 48 × 4 µm/0.48 µm, PM3: 3 × 4 µm/0.12 µm*

Once V_{DDi} reaches 600 mV, the peripheral circuits start to work. Second CSRO-2 provides a clock of 40 µs at 600 mV for the $L_{CNV1,2}$, and using control logic, complementary clocks (CLK and CLKbar) were generated to drive the switches NM-1, 2. A zero-current switching (ZCS) network generates two pulses (V_p and $V_p$bar) to close and open the switches PM-1, 2, according to the state of art mentioned in [3]. In ZCS, we have 16 delays in the range of 0.5–2.5 µs to cover the 50–200 mV of the TEG voltage, maintaining the required voltage resolution. The sequential search algorithm was used to choose one of the delays, according to the rising or falling edge of the $V_{SWD1,2}$ polarity, with respect to the pulse V_P/V_{Pbar} [3]. After boosting V_{OUT} from 600 mV to 1 V, the switch S_L is closed. In our design, the inductors are energised separately for two cycles of the clock pulses as shown in Fig. 3. Using this technique, we can extract more than 50% of the maximum available power from the TEG, without using any input capacitance C_{IN} in V_{IN} node of Fig. 1. Reference voltages are generated at V_{DDi} and V_{OUT} nodes and to regulate the power. The output voltage is regulated close to 1 V. Fig. 4 shows the picture of the die realising our proposed circuit.

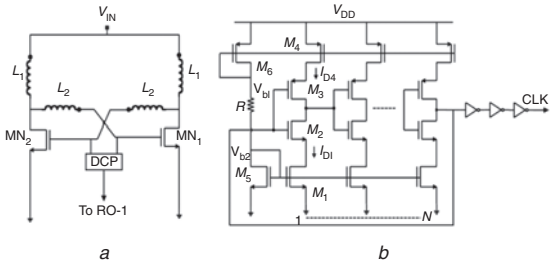

Fig. 2 *Circuit schematic for low voltage starter*

a LVS block showing ESRO + DCP. $MN_{1,2}$ are zero V_t transistors
b CSRO circuit configuration, $R = 8$ MΩ is on chip

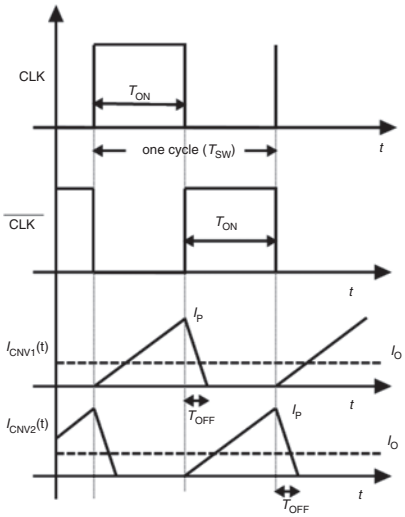

Fig. 3 *Clock scheme to control switches, NM1, PM1, NM2 and PM2. Figure also shows charging and discharging of currents through inductors L_{CNV1} and L_{CNV2}. Switches PM1 and PM2 are closed for T_{OFF} period. Duty cycle $D_2 = T_{OFF}/T_{SW}$*

Selecting inductors for ESRO, auxiliary and main stage

$$\frac{g_{ms}}{g_{md}} - \left(1 + \left(1 + \frac{1}{g_{md} \cdot R_P}\right) \cdot \frac{1}{K+1}\right) > 0, \qquad f_O = \frac{1}{2\pi\sqrt{C_{net} L_P (K+1)}} \tag{1}$$

The minimum startup voltage and oscillation frequency are two criteria to select the inductors for enhanced swing ring oscillator (ESRO) shown in Fig. 2. Equation (1) can be used to determine this criteria [4]. In (1), g_{ms}/g_{md} is extracted for $MN_{1,2}$ ($W/L = 6 \times 40 \times 4$ µm/0.42 µm) and its value is 1.57 at 30 mV, $K = L_2/L_1$, and R_P and L_P are the parallel equivalent of L_1, C_{net} is the equivalent capacitance at the gate of MN_1 and MN_2 and is 18 pF. The chosen value of $L_1 =$ 0.47 mH ($R_P = 260$ kΩ at 1 MHz) and $K = 5$ can give an oscillation frequency $f_o = 650$ kHz sufficient for the functioning of DCP. With this value of inductors, the ESRO starts to oscillate at 30 mV, but can only drive a CSRO when input reaches 50 mV.

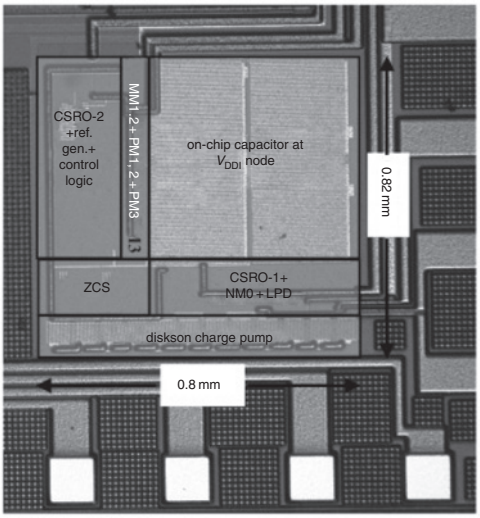

Fig. 4 *Photograph of die implementing circuit of Fig. 1*

The output power (P_O) available to the load is $I_O \times V_O$ [5], and can be expressed as

$$P_O \approx \left(\frac{V_{TEG}}{R_{EQ}}\right)^2 \left(1 - \exp\left(-\frac{T_{ON} R_{EQ}}{L}\right)\right)^2 \frac{L}{2 \cdot T_{SW}}. \quad (2)$$

In (2), $R_{EQ} = R_{SW} + R_{IND} + R_{TEG}$, R_{IND} is the internal resistance of the inductor, and R_{SW} is the resistance of the switch. For the main stage, (2) can be multiplied by 2, when the inductor is energised for both halves of a cycle shown in Fig. 3. Fig. 5 shows the plot of (2).

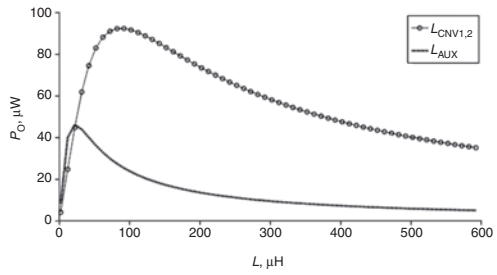

Fig. 5 *In plot, we have used $R_{SW} = 0.5\ \Omega$, $R_{IND} = 0.6\ \Omega$, $R_{TEG} = 5\ \Omega$ and $V_{TEG} = 50$ mV. $L_{CNV1,\ 2} = 100\ \mu$H can extract maximum power and $L_{AUX} = 560\ \mu$H can power the peripherals (4 µW at 1 V)*

Measurement results: To measure the response of the chip, we have used a source unit and a 5 Ω resistance in series. The setup was used to emulate the model from a Tellurex TEG, which has a sensitivity of 25 mV/K [2]. The value of the external components used are: C_{OUT} = 26 nF, $L_{CNV1,2}$ = 100 µH, L_{AUX} = 560 µH, ESRO: L_1 = 0.47 mH, L_2 = 2.2 mH. In the output, a variable potentiometer R_{OUT} = 0–50 kΩ was connected as a load, and the measurements were recorded. The definition of efficiency (i.e. η) used in this work is given by

$$\eta = \frac{P_{OUT}|_{V_{OUT}=1V}}{V_{TEG}^2/4 \cdot R_{TEG}} \times 100\% \quad (3)$$

In (3), V_{OUT} is the voltage across the load, which in our work is nearly equal to 1 V. However, this voltage will depend on the reference generator susceptibility to process variation. The efficiency varies from 60 to 65% at 50 and 200 mV, respectively. In Fig. 5, with lossless converter and no power consumption, a 90 µW power can be obtained. A power of 4 µW (at 1 V) is consumed by the auxiliary circuit. After transient loss, we are able to obtain 75 µW of power, which corresponds to 60% of the efficiency.

Fig. 6 shows the response of the chip for 50 mV input voltage, Ch2 (trace in light blue) corresponds to V_{DDi} and Ch1 (trace in blue) corresponds to V_{OUT}. The figure indicates that the V_{DDi} and V_{OUT} closes at 600 mV and the output is boosted to 1 V, and then the output is regulated close to 1 V. This clearly demonstrates the working of the prototype chip. Also a transient settling time <5 ms is achieved, which is a considerable improvement over the past work (see Table 1).

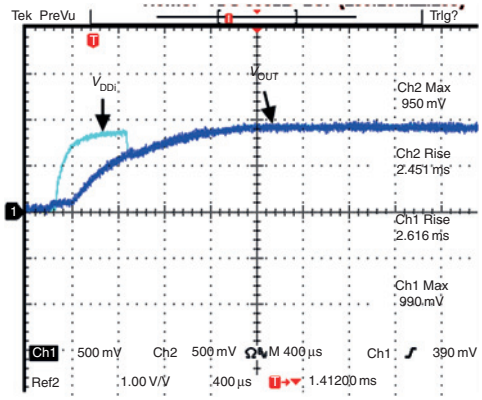

Fig. 6 *Transient response when $V_{TEG} = 50$ mV*

Table 1: Performance comparison

	Transient time (ms)	Startup voltage (mV)	Efficiency (%)	CMOS technology (nm)
[1]	18	35 mV (mechanical switch)	58 (end to end)	350
[3]	20	50 mV (self-starting)	73 (peak)	65
This work	3	50 mV (self-starting)	65 (peak)	130

Conclusion: A fully electrical energy harvester for a TEG, implemented in 130 nm CMOS process is presented. The measurement result shows that at 50 mV, transient settling time <5 ms, with peak efficiency of 65% and 50 mV startup is achieved.

Acknowledgments: The authors express gratitude to MOSIS for fabricating the circuit, under the MEP research program and to CNPq-CAPES for financing this project.

Submitted: *8 December 2015* E-first: *14 March 2016*
doi: 10.1049/el.2015.4263
One or more of the Figures in this Letter are available in colour online.

A.K. Sinha and M.C. Schneider (*LCI-CTC, Federal University of Santa Catarina, Santa Catarina, Florianopolis 88040-900, Brazil*)

✉ E-mail: arun.kumar.sinha@unige.it

References

1 Ramadass, Y.K., and Chandrakasan, A.P.: 'A batteryless thermoelectric energy harvesting interface circuit with 35 mV startup voltage', *IEEE J. Solid State Circuits*, 2011, **46**, (1), pp. 333–341
2 Ramadass, Y.K.: 'Energy processing circuits for low-power applications'. PhD dissertation, Massachusetts Institute of Technology, Cambridge, MA, 2009
3 Weng, P.S., Tang, H.Y., Ku, P.C., and Lu, L.H.: '50 mV-input batteryless boost converter for thermal energy harvesting', *IEEE J. Solid State Circuits*, 2013, **48**, (4), pp. 1031–1041
4 Machado, M.B., Schneider, M.C., and Montoro, C.G.: 'On the minimum supply voltage for MOSFET oscillators', *IEEE Trans. Circuits Syst.*, 2014, **61**, (2), pp. 347–357
5 Rogers, E.: Understanding boost power stages in switch mode power supplies. Application report, Texas Instrument, 1999